< DE/EJ/ET/EN/EX/EQ/IE/IS/IC >:<22636>: <Emerging Trends in Electronics>: <Advance Processors>: < UO1a.3 Write advantages of Pipelining technique >: <Assessments>: <Formative>

<Mr Pramod Menase>

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| Set 1: Question No 1 | Set 1: Question No 2 | Set 1: Question No 3 |
| \_\_\_\_\_\_\_\_\_\_ is a technique for implementing [instruction-level parallelism](https://en.wikipedia.org/wiki/Instruction-level_parallelism) within a single processor. | \_\_\_\_\_\_\_ is not the part of 3 stage pipelining. | Pipelining attempts to keep every part of processor\_\_\_\_\_\_. |
| Recall/ Remembering | Understanding | Application |
| 1. pipelining | 1. Fetch | 1. free |
| 1. arithmetic | 1. Decode | 1. busy |
| 1. logical | 1. Execute | 1. idle |
| 1. prediction | 1. Power | 1. lazy |
| Ans: < a > | Ans: < d > | Ans: < b > |

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| Set 2: Question No 1 | Set 2: Question No 2 | Set 2: Question No 3 |
| Following is not an advantage of pipelining. | Pipelining increases the \_\_\_\_\_\_\_\_\_\_\_\_\_ of the CPU. | To increase the speed of memory access in pipelining, we make use of \_\_\_\_\_\_\_ |
| Recall/ Remembering | Understanding | Application |
| 1. Instruction throughput increases | 1. memory | 1. Special memory locations |
| 1. Faster ALU can be designed | 1. power | 1. Special purpose registers |
| 1. Increases the overall performance | 1. overall performance | 1. Buffers |
| 1. CPU's works at lower clock frequencies | 1. size | 1. Cache |
| Ans: < d > | Ans: < c > | Ans: < d > |